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An Efficient 8-bit Wallace Tree Multiplier using 4:2 Compressor with CNTFET 32nm Technology

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***Abstract*—Multiplication is a critical operation in a wide range of Digital Signal Processing (DSP) applications, yet multipliers typically demand higher silicon area, incur significant latency, and consume greater power compared to other digital building blocks. To address these challenges, compressor-based architectures are widely adopted, as compressors play a pivotal role in the Partial Product Reduction (PPR) stage by enabling parallel accumulation and minimizing the number of intermediate product terms. This work presents an optimized compressor design integrated into a Wallace tree 8-bit multiplier to enhance computational efficiency. The Wallace tree structure, known for its parallel reduction capability, leverages the proposed compressor to achieve high speed and area-efficient multiplication. Carbon Nanotube Field Effect Transistor (CNTFET) technology, derived from advancements in Fin Field-Effect Transistor (FinFET) architectures, is employed due to the superior electrical conductivity and mechanical strength of carbon nanotubes. The proposed compressor exhibits reduced structural complexity and better regularity when compared with conventional designs. The Wallace tree 8-bit multiplier incorporating the new compressor is modeled and simulated using Cadence's Virtuoso tool with 32 nm CNTFET technology. Comparative simulation results demonstrate that the proposed design significantly reduces delay and power dissipation while improving speed, thereby outperforming conventional Wallace tree and compressor-based multiplier architectures.**

Keywords—Binary, CNTFET, VLSI and Multiplier

I. INTRODUCTION (*HEADING 1*)

Very high Scale Integration (VLSI) is the process of integrating a high number of transistors onto a single silicon microchip [1]. As more transistors were included into semiconductor circuits, this technology developed from small-scale integration (SSI). Developing low-power systems through the use of precise and effective power estimation algorithms is the core area of research in this field. Multiple components can be integrated into a single chip thanks to VLSI [2]. VLSI technology has several benefits, including reduced circuit size, increased operational speed, reduced power usage, and reduced cost. VLSI frequently uses a system-on-a-chip (SoC) design technique to do this [3]. Emerging nano electronic devices known as Carbon Nanotube Field-Effect Transistors (CNTFETs) use semiconducting carbon nanotubes as the channel material rather than silicon. They have exceptional electrical characteristics, including superior electrostatic control, ballistic transport, and high carrier mobility. Compared to traditional MOSFETs, these characteristics allow CNTFETs to achieve higher ON current, lower OFF current, and improved scalability, especially in low-nanometer technologies [4, 5]. Notwithstanding their benefits, the production of CNTFETs is fraught with difficulties, such as the need to precisely regulate the chirality of the nanotubes, precisely align and position the CNTs on the wafer, and reduce contact resistance. CNTFETs are positioned as a possible contender for expanding Moore's law and allowing next-generation high-speed, low-power devices because of this compatibility and their exceptional performance [4]. Carbon Nanotube Field-Effect Transistors (CNTFETs) perform better than FinFETs and nanowire FETs in terms of energy efficiency and decreased short-channel effects. CNTFETs have different performance characteristics from traditional MOSFETs because they use a carbon nanotube (or an array of nanotubes) as the channel substrate [6, 7]. A CNTFET's electrical characteristics are heavily impacted by the diameter and chiral angle of the nanotube, which determine its bandgap, whereas only a small percentage of the heat produced within the device is dissipated through the channel. Carbon nanotubes may emerge as a top contender for next-generation nanoscale transistor devices if these characteristics are successfully utilized [8]. Theoretically, carbon nanotubes have thermal conductivity similar to that of sapphire or diamond, and because of their nanoscale size, they can switch more quickly and reliably while using a lot less power than conventional silicon-based devices. Many of these issues can be resolved with continued technical development, hence bolstering Moore's law [9]. Digital Signal Processing (DSP) devices are essential components of portable computers that run on rechargeable batteries due to their small size, excellent performance, and low power consumption. They are the perfect computer platform for multimedia and image processing applications because of these characteristics [10]. One of the most important parts of the arithmetic block in a DSP system is the multiplier [11]. Typically, a multiplier works in three stages: Partial Product Generation (PPG), in which the multiplier and multiplicand bits are ANDed to create partial product operands; Partial Product Reduction, in which the partial product terms are reduced into two operands using a 4:2 compressor; and Carry Propagate Addition (CPA), in which the two reduced operands are added to get the final result [12–14]. As shown in Fig. 4, two traditional full adders are cascaded to generate the 4:2 compressor (Existing Model 1). In addition to a carry

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input from a lower significant location, this design takes four binary inputs [15]. In order to achieve carry-free compression, the compressor produces the primary sum and carry outputs in addition to the carry to the next binary position [16, 17]. One full adder, two pseudo-half adders (HA+), and a two-input NOR gate make up the compressor's pseudo-half adder circuitry (Existing Model 2) [18]. In contrast to the traditional 4:2 compressor, this design uses a NOR gate and two pseudo-half adders in place of one full adder. Therefore, to accomplish the necessary compression, the design makes use of pseudo-half adders and a NOR gate rather than just conventional full adders [19]. Existing Model 3 uses a majority gate and four XOR gates to implement the compressor. The design is based on the standard 4:2 compressor structure, which usually uses cascaded full adders, but in contrast to the conventional method, the Boolean functions of the full adder are restructured and realized using 3-input majority gates and 2-input XOR gates [20]. In order to reduce or eliminate the final negative signal in the partial product row, a novel technique that helps minimize overall design delay is used in the design of the proposed 4:2 compressor. This modification is integrated into the logical circuit of the 4:2 compressor, which uses an inverter, a 2×1 multiplexer, five NAND gates, two XNOR gates, one OR gate, one XOR gate, and an inverter. Simulations are then conducted to assess the performance of the design in terms of transistor count, power dissipation, and latency, and the results are compared with existing models to validate improvements in performance metrics. The structure of the paper is as follows: The basic 4:2 compressor design and an overview of relevant literature-based models are presented in Section 2. A thorough explanation and analysis of the suggested model are given in Section 3. The effectiveness of the suggested designs is assessed in Section 4 by contrasting the outcomes of simulation and synthesis with those of more contemporary models. The article ends by summarizing its main conclusions and suggesting possible paths of inquiry for further study.

II. Existing Design and Its Methodologies

A. *Traditional4:2 compressor design using two full adders*

Two complete adder circuits are used in the design of the conventional 4:2 compressor [21]. Four binary inputs are accepted by it: x i) in addition to the lower significant bit's carry input [22]. By producing the primary carry and sum outputs in addition to the carry propagated to the subsequent binary position (C out), this device accomplishes carry-free compression. Equation (1) expresses the 4:2 compressor's output:

$$Cout = Majority [x1+x2+x3] \ldots\ldots\ldots (1)$$

Figure 1 illustrates the structure of the 4:2 compressor, which is implemented using two cascaded full adders. The circuit consists of four inputs (x1, x2, x3, x4) and two primary outputs: Sum and Carry. Additionally, the output Cout serves as the carry input (Cin) for the next higher-order stage. Importantly, Cin and Cout operate independently, as expressed in Eqs. (2) and (3), thereby confirming the carry free nature of the compressor. This existing model requires a total of 56 transistors.

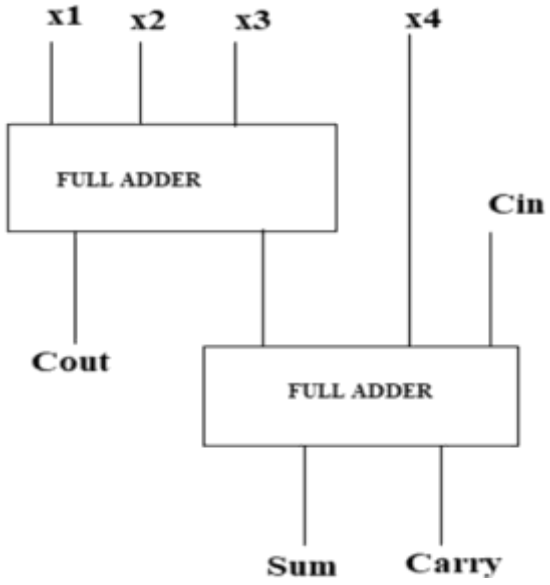

Fig. 1 Representation of 4:2 compressor using two full adders

$$Sum=x1\oplus x2\oplus x3\oplus x4\oplus Cin \ldots\ldots\ldots\ldots (2)$$

$$Carry=Majority [(x1\oplus x2\oplus x3), x4, Cin] \ldots\ldots. (3)$$

B. *4:2 compressor design using 2:1 multiplixer*

The conventional 4:2 compressor's design is the main topic of this section. The research describes the fundamental ideas and procedures of binary multiplication in addition to the difficulties brought on by multipliers' excessive power consumption. To optimize the design, a new approach for lowering the last negative signal in the partial product row is introduced. To assess the enhancements, a power performance comparison is also given.

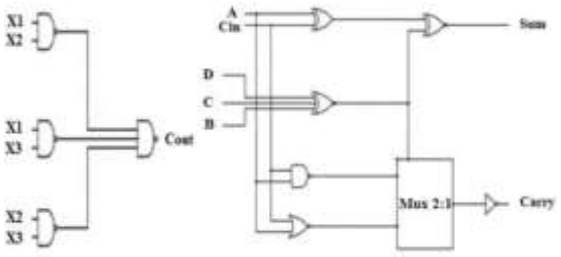

Fig. 4 Schematic view of 4:2 compressor using 2:1 mux

The proposed 4:2 compressor concept is shown in Figure 4. Table 1 displays the output table for this compressor, which was constructed with a CNTFET at 0.9 V. The Sum and Carry outputs are produced by the design using a total of 56 transistors. Other logic gates, such NAND and XNOR, are effectively optimized by the 32nm CNTFET architecture without requiring more space or complexity. Furthermore, notable decreases in latency and power consumption are made possible by CNTFETs' superior electrostatic control and great carrier mobility. The tool-generated representation of the suggested compressor is displayed in Figure 5, and Equations 5, 6, and 7 contain the Sum, Carry, and Cout equations.

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Sum = (A ⊕ Cin) ⊙ (D ⊙ C ⊙ B) …….. (5)
Carry = (D⊙ C ⊙B) . (A +Cin) + (D⊙ C ⊙B).(A .Cin) … (6)
Cout = ((B . C) . (B . D) . (C . D)) …… (7)

A multiplexer is a combinational circuit that selects one output from multiple inputs. With *n* selection lines, a multiplexer can accommodate 2n input combinations [30]. Among the different types of multiplexers, the proposed design employs a 2 × 1 multiplexer. This configuration consists of two inputs (D0 , D1), a single selection line (S), and one output (Y). The logical expression for the 2 × 1 multiplexer is given in Equation 8,

Y=D0.S+D1.S …….. (8)

An effective 4:2 compressor model is created and put into practice in this study by substituting a 2 × 1 multiplexer for a three-input majority gate. Basic logic gates process the inputs A, B, C, D, and Cin to yield the outputs Sum, Carry, and $Cout$. The design was examined at various supply voltages between 0.7 and 1.1 volts. Four NAND gates are used to create $Cout$.

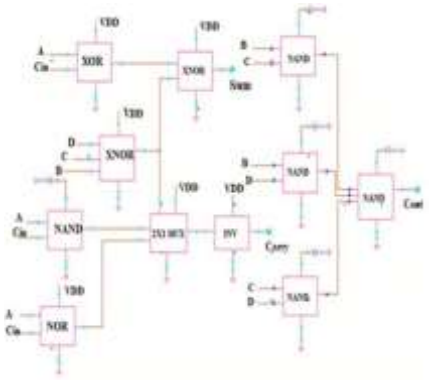

Fig. 5: Tool view of 4:2 compressor using 2:1 mux

C. 4:2 Compressor design using three input majority gate

In multiplier design, energy-delay trade-offs and circuit implementation techniques are crucial. It is necessary to carefully evaluate multiplication algorithms, technological limitations, and implementation strategies while creating an energy-efficient parallel multiplier. Circuits' energy efficiency and dependability can be improved by utilizing several logic structures instead of just XOR-based techniques [26]. However, a notable decrease in performance is frequently seen in newer technologies that use majority logic- based XOR, AND, and OR gates.

The simplest basic technique for creating partial products is the AND operation. Although it involves more sophisticated partial product generation, the Booth algorithm is frequently used to decrease the number of partial products. Additionally, this technique makes it easier to create negative partial products, which need two sign bits to function properly. A number of strategies have been put forth over time to quicken the second stage of partial product reduction (PPR).

The number of partial products in an array multiplier is inversely proportional to the latency. There are 48 transistors in the current model. Higher-order compressors can further reduce delay, while three-dimensional optimization approaches can further reduce delay by matching fast outputs with delayed inputs for better performance. A 4:2 compressor that uses a three-input majority gate is shown in Figure 3 [27]. When at least two of a majority gate's three inputs are true and each input contributes equally to the outcome, the gate's output is true. Any two input relationships can be compared to the majority function thanks to this design [28]. In particular, the gate generates a true output when two or more inputs are active, and a false output when none or just one input is active. Equation (4) expresses the logic function of a three-input majority gate as follows:

M (j, k, l) = j ∗ k+k ∗ l+ l ∗ j …….. (4)

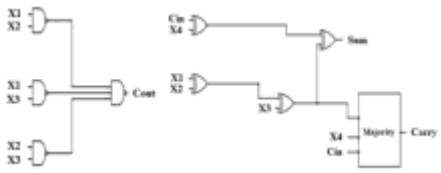

Fig.3 Representation of 4:2 compressor using three input majority gate

The Cadence Virtuoso EDA tool was used to implement the compressors in this section. Two traditional half adders were used in the design of the initial model that was created. The third extant model was built using a three- input majority gate, whereas the second model used pseudo- half adders in conjunction with a full adder [29].

III. PROPOSED DESIGN

As shown in Figure 2, the 4:2 compressor in this model is designed with a NOR gate, a full adder, and a pseudo half adder. In contrast to the traditional compressor, this design uses a NOR gate and two pseudo half adders in place of one full adder. 4:2 compressors have drawn a lot of interest because they allow structural regularity in VLSI systems, especially for their function in 2:1 reduction [23]. Additionally, by adding a few NOT gates to the 4:2 compressor structure, Row Bypassing Adders—which use a binary-signed digit number system to express partial products—can be effectively implemented in parallel binary multiplication systems. These extra NOT gates can be removed by using inverted megabit encoding, which enables 4:2 compressors to be used directly in place of RBAs. NOR gates are frequently chosen over XOR gates in CMOS circuitry due to their shorter delay. It is possible to methodically create NOR-based 4:2 compressor topologies by integrating the necessary carry full adder. An OR gate is used to generate the carry output in the pseudo-half adder circuit, and an XNOR gate is used to obtain the sum output [24, 25].

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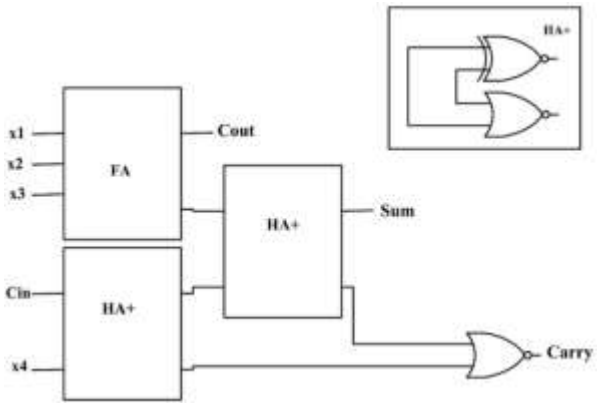

Fig. 2 Representation of proposed 4:2 compressor using pseudo half adders

Table 1 Truth table of the proposed 4:2 compressor at 0.9V

A	B	C	D	Cin	Sum	Carry	Cout
0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0
0	0	0	1	0	1	0	0
0	0	0	1	1	0	1	0
0	0	1	0	0	1	0	0
0	0	1	0	1	0	1	0
0	0	1	1	0	0	0	1
0	0	1	1	1	1	0	1
0	1	0	0	0	1	0	0
0	1	0	0	1	0	1	0
0	1	0	1	0	0	0	1
0	1	0	1	1	1	0	1
0	1	1	0	0	0	0	1
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	0	1	1
1	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	0	0	1	0
1	0	0	1	1	1	1	0
1	0	1	0	0	0	1	0
1	0	1	0	1	1	1	0
1	0	1	1	0	1	0	1
1	0	1	1	1	0	0	1
1	1	0	0	0	0	1	0
1	1	0	0	1	1	1	0
1	1	0	1	0	1	0	1
1	1	0	1	1	0	0	1
1	1	1	0	0	1	0	1
1	1	1	0	1	0	0	1
1	1	1	1	0	0	1	1
1	1	1	1	1	1	1	1

IV. Overview of an 4:2 Compressor Using 8-Bit Wallace Multiplier

A 4:2 compressor is an efficient digital circuit used in multipliers, particularly in Wallace tree multipliers, to speed up the partial product reduction stage by reducing four input bits and two carry bits into two output bits without carry propagation to the next stage. This compressor's carry-free nature enhances speed and reduces delay, making it highly suitable for high-performance multipliers. In the context of an 8-bit Wallace tree multiplier, 4:2 compressors are used to compress the partial product bits generated during multiplication. The Wallace tree structure uses successive layers of compressors (including 4:2 and 3:2 compressors) to reduce the partial products into just two operands. These two operands are then summed by a fast adder to produce the final product. The 4:2 compressor can be designed using XOR gates and multiplexers to optimize delay and power consumption.

The Wallace tree multiplier employing 4:2 compressors significantly enhances speed and area efficiency compared to conventional array multipliers or Wallace multipliers using only 3:2 compressors. Simulation results show that such multipliers achieve lower delay (for example, in nanoseconds), reduced power consumption, and smaller area overhead, making them suitable for VLSI implementations in DSP applications. This approach of combining 4:2 compressors within an 8-bit Wallace tree multiplier architecture results in an efficient, high-speed multiplication suitable for advanced technologies like 32 nm CNTFET or FinFET.

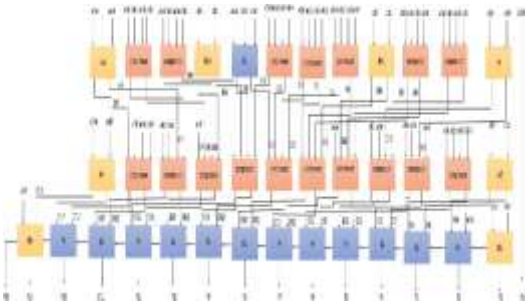

Fig. 6: Using 4:2 compressor to construct 8-bit Wallace tree multiplier

The output waveform of a 4:2 compressor in the context of an 8-bit Wallace tree multiplier represents the time-domain behavior of the compressor's outputs relative to its inputs during the multiplication process.The 4:2 compressor takes four main input bits and two carry bits (carry-in, carry from a previous compressor stage, and carry- out to the next stage) and generates two outputs: a sum output and a carry output. These outputs represent the condensed partial products needed for the Wallace tree reduction.

The waveform typically shows the following:

- Input signals (four partial product bits plus carry-in)
- Output sum signal
- Output carry signal
- Timing relationships indicating how quickly the compressor produces stable outputs after inputs change

In published waveforms for 4:2 compressors, the sum and carry outputs transition asynchronously but stabilize shortly after the inputs change, indicating delay and propagation time of the compressor circuit. This is crucial for assessing the speed of the Wallace tree multiplier as these compressors reduce the number of partial products efficiently.

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For specific waveforms, simulation tools like Cadence Virtuoso are often used to generate transient response plots showing input pulses and corresponding output transitions. The sum and carry outputs are complementary and timed to prevent carry propagation delay bottle necks. If a waveform image or simulated plot of the 4:2 compressor outputs within an 8-bit Wallace tree multiplier is needed, these can be generated through digital circuit simulation in tools such as Cadence Virtuoso with CMOS or CNTFET transistor-level designs.

V. Results and Discussion

Cadence software was used for the design and simulation of the suggested and current approaches. Through the simulations, important performance measures such as dynamic power, latency, EDP, and PDP were assessed. Table 2 provides a summary of the CNTFET model parameters used in this investigation.

Simulation result and parameters analysis of traditional 4:2 compressor using two complete full adders

A. *Simulation results and parameters analysis of traditional 4:2 compressor using two complete full adders*

The operating voltage of 0.9 V is applied to the input pins, and the output waveform is obtained from the Carry and Sum. The resultant waveform is shown in Fig. 6, and the propagation delay factor and the EDP and PDP values for varying voltages from 0.7 to 1.1 V. Due to the increase in the biasing voltage, the power and delay values also increase. In the waveform, A, B, C, D, and CIN are the five inputs for the compressor, and the variables X and Y represent sum and carry, respectively. Other than sum and carry, another output called COUT is obtained. it is found that the propagation delay value is approximately equal at various values between

0.7 and 1.1 V. Increased power and delay values result in increased PDP and EDP values.

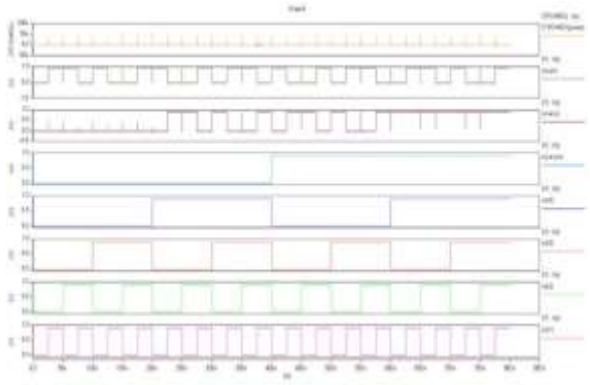

Fig: Simulation Result and Parameters of 4:2 Compressor Using Two Full Adders.

B. *Simulation result and parameters analysis of 4:2 compressor design*

The resultant waveform as shown in Fig. 9. The performance analyses are tabulated in Table 5. In the waveform, A, B, C, D and Cin are the five inputs for the compressor, and the variables X and Y represent sum and carry, respectively**.** Other than sum and carry, another output called COUT is obtained. From the Table 6, it is found that the propagation delay value is constant at various voltage values between 0.7 and 1.1 V.

Increased power values result in increased PDP and EDP values. Comparing the power and propagation delay values of the existing models 1, 2 and 3, the output result obtained for the proposed 4:2 compressor using a 2 × 1 multiplexer is comparatively
low

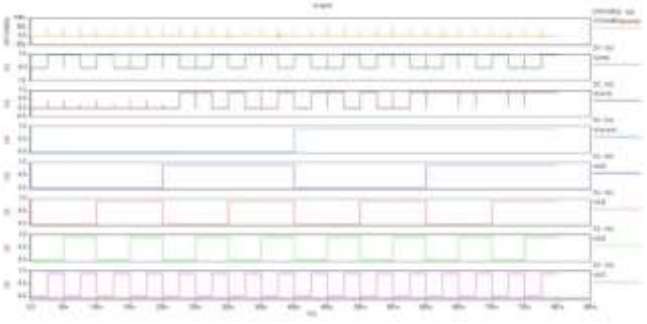

Fig. 8: Simulation result and parameters analysis of 4:2 compressor desin

C. *Simulation result and parameter analysis of 4:2 compressor using three input majority gate*

The operating voltage of 0.9 V is applied to the input pins, and the output waveform is obtained from the Carry and Sum. The output waveform is shown in Fig. 8. The performance metrics various voltage values between 0.7 and

1.1 V. Due to the increase in the supply voltage, the power and delay values also increase. In the waveform, A, B, C, D and Cin are the five inputs for the compressor, and the output variables are represented by Sum, Carry, and Cout, respectively. It is found that the propagation delay value is approximately equal at different voltages. Increased power and delay values result in increased PDP and EDP values. Comparing the power and propagation delay values of the existing models 1 and 2, the output result obtained for the 4:2 compressor using a three-input majority gate is comparatively low.

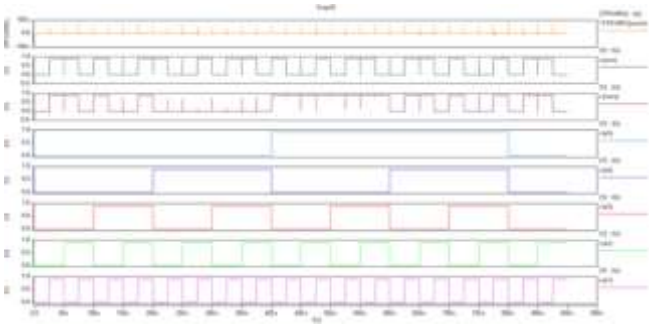

Fig. 9: Simulation result and parameter analysis of 4:2 compressor using three input majority gate

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D. Simulation result and parameter analysis of proposed 4:2 compressor using two pseudo half adders

The operating voltage of 0.9 V is applied to the input, and the resultant waveform is obtained from Carry and Sum. The output waveform is shown in Fig.7.The performance metrics are tabulated in Table 3 at various

values between 0.7 and 1.1 V. Due to the increase in the supply voltage, the power and delay values also increase. In the waveform, A, B, C, D and Cin are the five inputs for the compressor, and the output variables are represented by Sum, Carry, and Cout, respectively. From the Table 4, it is found that the propagation delay value is approximately equal at various values between 0.7 and 1.1 V. Increased power and delay values result in increased PDP and EDP values

Comparison of performance metrics among existing and proposed model

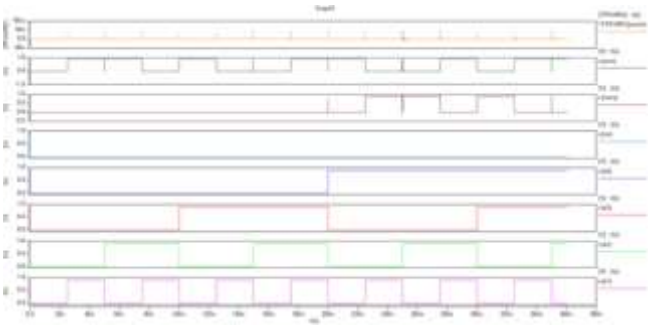

Fig: Simulation Result and Parameter Analysis of Proposed 4:2 Compressor pseudo half adder

Table 7 represents the comparison among the models. The performance metrics have been analyzed. The average values of the obtained results of existing and proposed models are tabulated. The table confirms that the proposed structure is more effective than the methods currently in use. From the graphs of power, delay, PDP, and EDP, it is found that the 4:2 compressor using two pseudo- half adders (existing model 2) shows a larger value comparatively than the other models. There are 68 transistors in the existing Model 2. An increased power value and output delay are caused by an increased transistor count.

Parameter	Power (nW)	Delay (ps)	PDP (fJ)	EDP (fJ·ps)
Existing-1 (FA)	305.68	12.464	3,810.8	47,480
Existing-2 (Pseudo HA)	39.73	7.8223	310.7	2,430
Existing-3 (4:2Compressor)	18,500	5.96	110,260	657,150
Proposed (3-bit Majority)	21.743	10.832	235.5	2,551

Partial product reduction stages. The 4:2 compressor efficiently compresses four input bits and one carry-in to two outputs, enabling faster accumulation of partial products with reduced delay compared to conventional full adder-based reduction techniques. This results in fewer stages in the Wallace tree, effectively decreasing the critical path and improving overall multiplier performance. Furthermore, the 4:2 compressor-based Wallace tree multiplier demonstrates reductions in power consumption and area, making it suitable for high-performance and low-power digital signal processing (DSP) applications.

VI. Conclusion

The implementation of an 8-bit Wallace tree multiplier using 4:2 compressors significantly improves the multiplier's speed and efficiency by reducing the number of partial product reduction stages. The 4:2 compressor efficiently compresses four input bits and one carry-in to two outputs, enabling faster accumulation of partial products with reduced delay compared to conventional full adder based reduction techniques. This results in fewer stages in the Wallace tree, effectively decreasing the critical path and improving overall multiplier performance. Furthermore, the 4:2 compressor-based Wallace tree multiplier demonstrates reductions in power consumption and area, making it suitable for high-performance and low-power digital signal processing (DSP) applications.

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